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The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1 - 46 (Previously Cancelled).

47. (Currently Amended) A nonvolatile semiconductor memory comprising:

- a first memory cell section including a first memory cell;
- a second memory cell section including a second memory cell;
- a first bit signal line connected to said first memory cell section;
- a second bit signal line connected to said second memory cell section, being different from said first bit signal line; and
- a latch circuit having a common node connected to one ends of said first and second bit signal lines;

wherein first program /read data of said first memory cell is latched in said latch circuit, while second program /read data of said second memory cell is held by said second bit signal line.

48. (Currently Amended) A nonvolatile semiconductor memory comprising:

- a first memory cell section including a first memory cell;
- a second memory cell section including a second memory cell;
- a first bit signal line connected to said first memory cell section;
- a second bit signal line connected to said second memory cell section, being different from said first bit signal line; and
- a latch circuit having a common node connected to one ends of said first and second bit signal lines;

wherein

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said first and second memory cells are programmed substantially simultaneously; and while said program voltage is supplied to said second memory cell, a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said latch circuit, and while said program voltage is supplied to said first memory cell, a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said latch circuit.

49. (Currently Amended) A nonvolatile semiconductor memory according to claim 48, wherein

while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second bit signal line, and

while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first bit signal line.

50. (Currently Amended) A nonvolatile semiconductor memory comprising:
a first memory cell section including a first memory cell;
a second memory cell section including a second memory cell;
a first bit signal line connected to said first memory cell section;
a second bit signal line connected to said second memory cell section, being different from said first bit signal line; and
a latch circuit having a common node connected to one ends of said first and second bit signal lines;

wherein

said first and second memory cells are programmed substantially simultaneously;

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while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second bit signal line, and while said program voltage is supplied to said second memory cell, the program data of said first memory cell held by said first bit signal line is latched in said latch circuit and a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said latch circuit;

while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first bit signal line, and while said program voltage is supplied to said first memory cell, the program of data said second memory cell held by said second bit signal line is latched in said latch circuit and a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said latch circuit.

51. (Original) The nonvolatile semiconductor memory according to claim 47, wherein

said first memory cell and said second memory cell are connected to different word lines.

52. (Original) The nonvolatile semiconductor memory according to claim 48, wherein

said first memory cell and said second memory cell are connected to different word lines.

53. (Original) The nonvolatile semiconductor memory according to claim 49, wherein

said first memory cell and said second memory cell are connected to different word lines.

54. (Original) The nonvolatile semiconductor memory according to claim 50, wherein

said first memory cell and said second memory cell are connected to different word lines.

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55. (Currently Amended) A nonvolatile semiconductor memory comprising:
a first memory cell section including a first memory cell;
a first bit signal line connected to said first memory cell section;
a second bit signal line, being different from said first bit signal line; and
a latch circuit having a common node connected to one ends of said first and second bit
signal lines latching program / read data;

wherein

said program / read data of said first memory cell is held by said second bit signal line.

56. (Currently Amended) A nonvolatile semiconductor memory comprising:
a first memory cell section including a first memory cell;
a first bit signal line connected to said first memory cell section;
a second bit signal line, being different from said first bit signal line; and
a latch circuit having a common mode connected to one ends of said first and second bit
signal lines, latching program / read data;

wherein

while a program voltage is supplied to said first memory cell, program data of said first
memory cell is held by at least one of said first and second bit signal lines;

after said program voltage is supplied to said first memory cell, said latch circuit is
electrically connected to said second bit signal line and the program data of said first memory cell
held by said second bit signal line is latched in said latch circuit; and

a verify read operation to verify whether said first memory cell has been sufficiently

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programmed, is carried out using said program data latched in said latch circuit.

57. (Currently Amended) A nonvolatile semiconductor memory comprising:

- a first memory cell section including a first memory cell;
- a first bit signal line connected to said first memory cell section;
- a second bit signal line;
- a second memory cell section including a second memory cell;
- a third bit signal line connected to said second memory cell section;
- a fourth bit signal line; and
- a latch circuit having a common node connected to one ends of said first, second, third and fourth bit signal lines, latching program/read data of at least one of said first and second memory cells;

wherein

- said first, second, third and fourth bit signal lines are different from each other;
- said first and second memory cells are programmed substantially simultaneously, program data of said first memory cell is held by at least one of said first and second bit signal lines, and program data of said second memory cell is held by at least one of said third and fourth bit signal lines while a program voltage is supplied to said first and second memory cells;

- a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out by said latch circuit, and program data of said second memory cell is held by said fourth bit signal line while conducting the verify read operation of said first memory cell; and

- said latch circuit and said fourth bit signal line are electrically connected to each other, after the program data of said second memory cell held by said fourth bit signal line is latched in said latch

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circuit, a verify read operation to verify whether said second memory cell has been sufficiently programmed, is carried out using the program data of said second memory cell held by said latch circuit, and while conducting a verify read operation of said second memory cell, the program data of said first memory cell is held by said second bit signal line.

58. (Previously Presented) The nonvolatile semiconductor memory according to claim 57, wherein

 said first and second memory cells are connected to a same word line.

59. (Currently Amended) The nonvolatile semiconductor memory according to claim 55, wherein

 while said program / read data is held by said first or second bit signal line, a potential of a bit signal line adjacent to said first or second bit signal line is set at a fixed potential.

60. (Original) The nonvolatile semiconductor memory according to claim 59, wherein

 said fixed potential is a ground potential or a power supply potential.

61. (Canceled)

62. (Currently Amended) The nonvolatile semiconductor memory according to claim 56, wherein

 while said program / read data is held by said first or second bit signal line, a potential of a bit signal line adjacent to said first or second bit signal line is set at a fixed potential.

63. (Original) The nonvolatile semiconductor memory according to claim 62, wherein

 said fixed potential is a ground potential or a power supply potential.

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64. (Canceled)

65. (Currently Amended) The nonvolatile semiconductor memory according to claim 57, wherein

while said program / read data is held by said first, second, third or fourth bit signal line, a potential of a bit signal line adjacent to said first, second, third or fourth bit signal line is set at a fixed potential.

66. (Previously Presented) The nonvolatile semiconductor memory according to claim 65, wherein said fixed potential is a ground potential or a power supply potential.

67-81. (Canceled)

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